HIGH-PERFORMANCE-SENSORSYSTEME durch Verbindung von Siliziumtechnologie und keramischer Mehrlagentechnik

HIPS | HIGH PERFORMANCE SENSORS

Powered by SiCer – The best of both worlds

IVAM Midweek Coffee Breack
Overview Part 1 HIPS Joint Research Project:

SiCer Technology Platform for Complex Sensors

Franz Bechtold e.a.

GEFÖRDERT VOM
UNTERNEHMEN REGION
Die BMBF-Innovationsinitiative Neue Länder
Bundesministerium für Bildung und Forschung

Content

- **Technology platform**
- **Current approach, partners**
- **Milestones on the road to success**
- **Milestone 1 and 2 results**
- **Highlights from the consortium**
- **Milestone 3 achievements**
- **Summary and conclusion**

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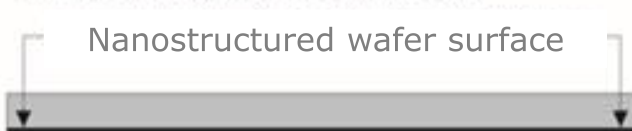
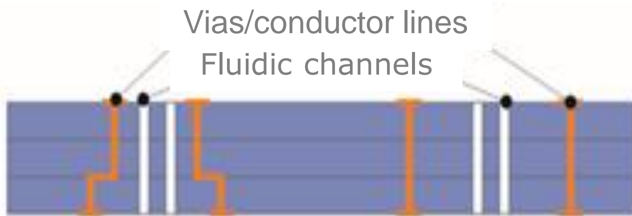
A silicon-LTCC composite substrate with special properties

The SiCer composite substrate is fabricated by sintering LTCC film onto a silicon wafer at 900°C.

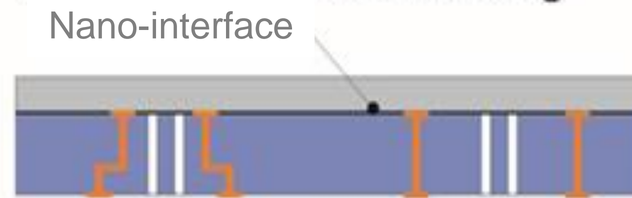
1. Etching the Si wafer



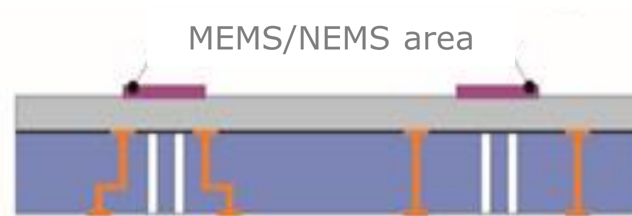
2. LTCC processing (green)



3. Lamination & Sintering



4. Thin-film processing



5. Separation by Si etching

6. Packaging & Singulation

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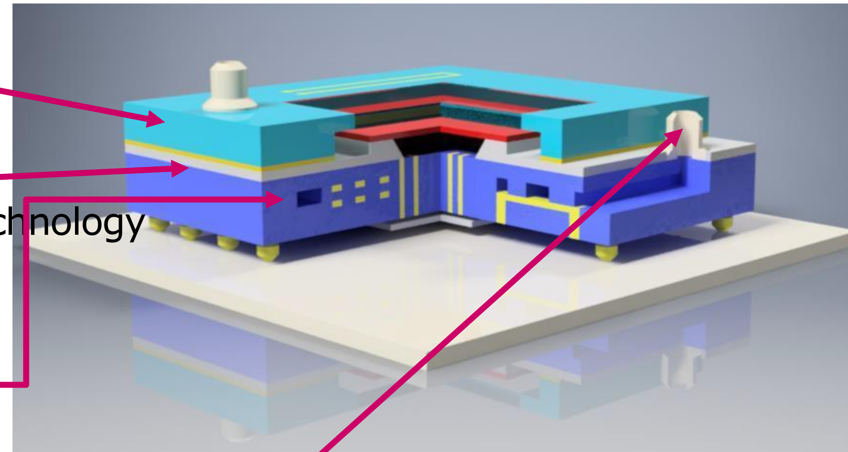
Illustration of the SiCer technology platform elements

- Topic 1: Materials
  - Eg. Glassceramics, Metallization, Functional layers
- Topic 2: Processes
  - Eg. Sintering, Assembly and Packaging technology
    - Topic 3.1 Structures
      - Eg. Membrane, Channel



- Topic 3.2: Features
  - Eg. Reaction chamber, Fluidic Interface

Partner
Fraunhofer IKTS (IKTS)
Technical University Ilmenau (TUIL)
University of applied science – Jena (EAH)
Micro-Hybrid Electronic GmbH (MHE)
VIA electronic GmbH (VIA)
IMMS GmbH (MMS)
CIS Forschungsinstitut (CIS)
5 microns GmbH (5M)
Siegert TFT GmbH (STFT)
Abatec Mikrosysteme GmbH (former LHT)
LLT Applikation GmbH (LLT)

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1. Process capability of the material system

- 1st generation tape with a thickness of 100 - 120µm ± 10% and sheet size of 4 "x4" is useable
- Compatibility of the commercial pastes for the basic processes are validated and is available
- Bonding of Si and Ceramic with low pressure assisted sintering is developed and validated
- SiCer basic process is feasible and validated at the partners' sites

2. System capability

- Interfaces for bonding and soldering processes are available
- Design rules for the Assembly and packaging technologies are available
- Bonding and soldering processes can be performed and are validated

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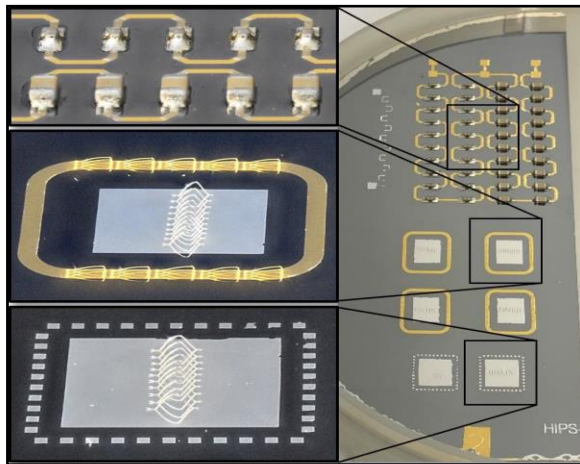
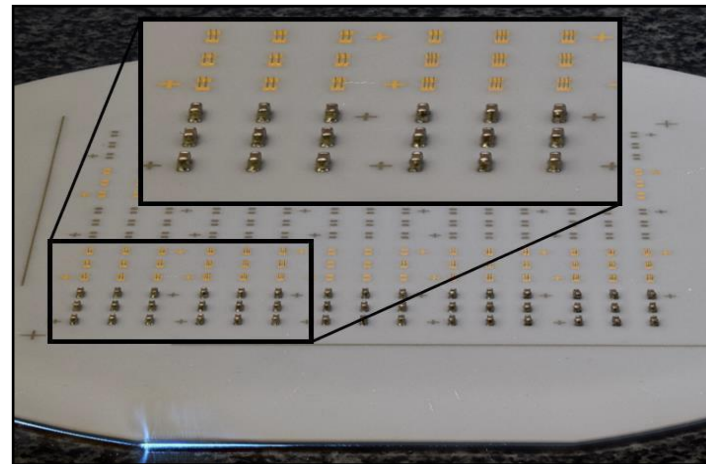
Assembly and packaging technology (AVT):

- Interface for the bonding and soldering are validated both on Si and LTCC side.
- Components have been successfully soldered and wire bonded in their respective soldering and wire bonding areas both on Si side and LTCC side.

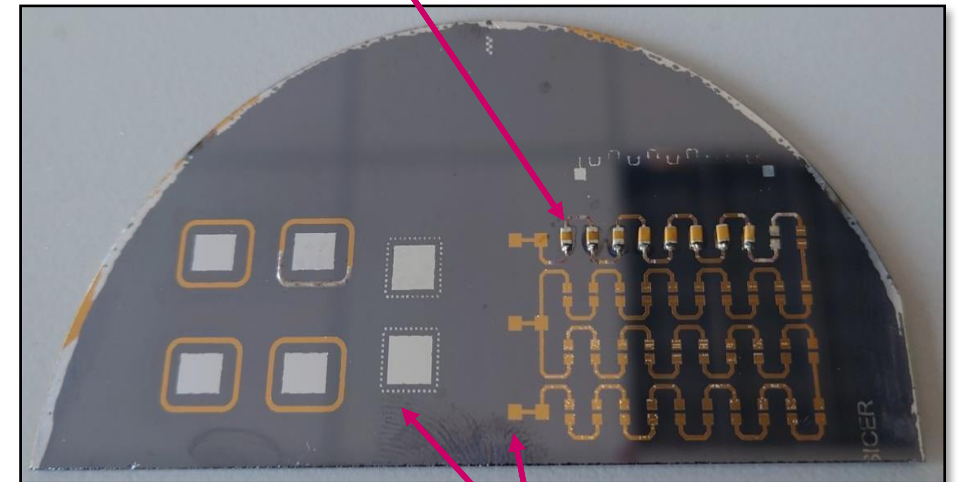


Silicon side
Sample Id: CK13_MS2_2



Ceramic side
Sample Id: CK13_MS2_9

Soldering interface – Si side



Bonding interface – Si side

Evaluated at 4 different partners: LHT, CIS, TUIL, MHE

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Results – Milestones 1 and 2

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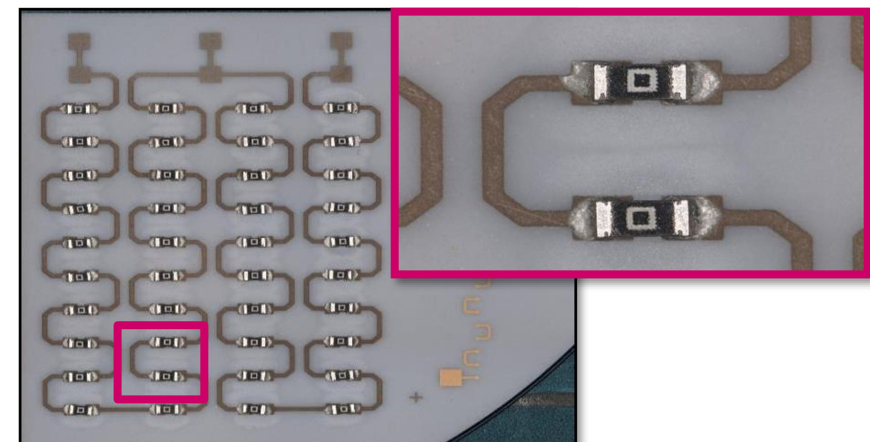
Assembly characterisation :


Daisy-chain structures with soldered SMD components

Vacuum-brazed Kovar caps: Left –Ceramic side; Right: Si side

Climate test - SiCer					
AVT	Substrates soldered LTCC side		Substrate Wire bonded (Alu 32 µm)	Substrates with hermeticity	
Material	Almit LFM48U MDA-5 (Jetter)	Koki SnAg3Cu7	Ceramic side	Kovar cap on Ceramic side	Kovar cap on Si side
Thermal shock test (-40 … +85°C; 100 cycles; Dwell time 30 min, Transition time 10s)	No abnormalities visible	No abnormalities visible	No abnormalities visible	-	No abnormali ties
Climate storage test (100,500,1000h at +85°C)	100h without abnormalities	100h without abnormalities	Upto 100h without abnormalities	-	-
Humidity storage test (85% humidity, 85°C, 168h)	Test in progress		Test in progress	Test in progress	

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Progress in the main topics

- **Material development: T**ape, pastes, functional materials
- **Process optimization: P**retreatment, laminating, cofiring, release tapes, sacrificial materials
- **Structural and demonstrator elements:** Cavities and channels
- **Integration of sensor and electrical functions:** electrostatic toolbox. NTC resistors
- **Process upscaling:** Tape casting, sheet size

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Highlights IKTS

Development of the BCT LTCC tape for SiCer manufacturing

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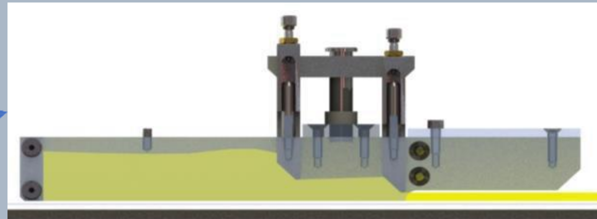
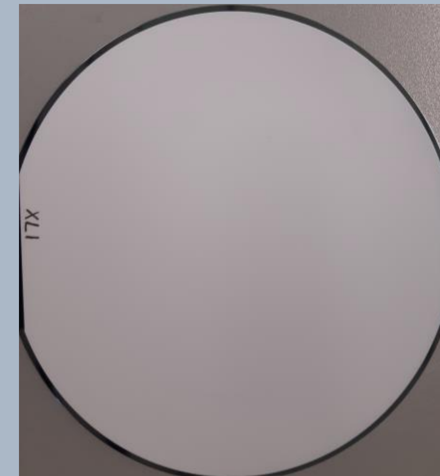
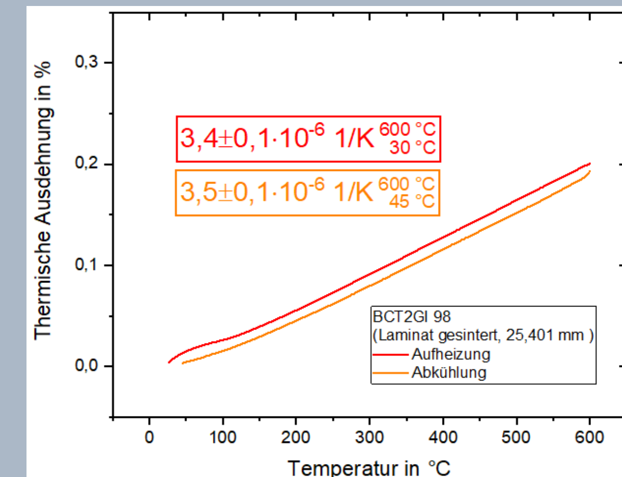
Upscaling:
- Development of continuous tape casting process to produce larger quantity of tape
- From the laboratory to the pilot production scale
- Adjustment of the casting parameters
  - Squeegee gap, casting speed, Casting box width
  - Temperature profile in the drying channel



Further development of the LTCC recipe

Adaptation of the CTE
- Casting the new film composition
- Test of the new film composition
- Coefficient of Expansion
  - Shrinkage
  - Density
  - Behaviour in SiCer-Process

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Highlights IKTS

Tailored Ag-metallization for the SiCer process

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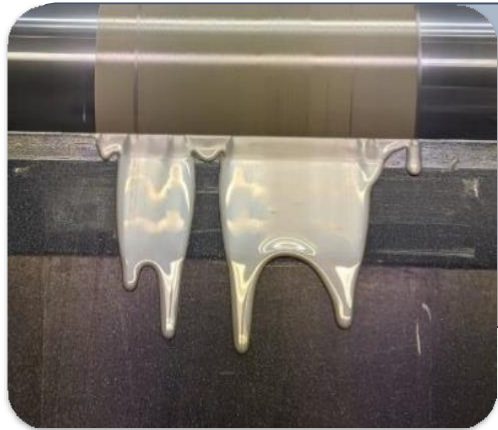
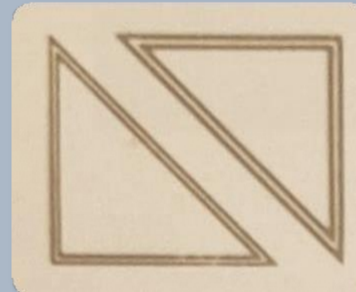
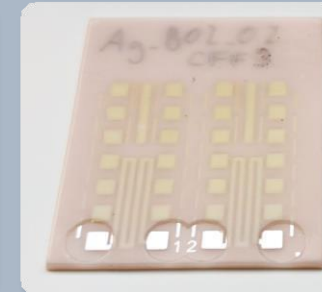
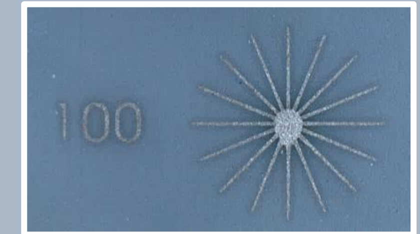


- Paste: Preparation and characterization
- Application dependent optimization

Conductor prints

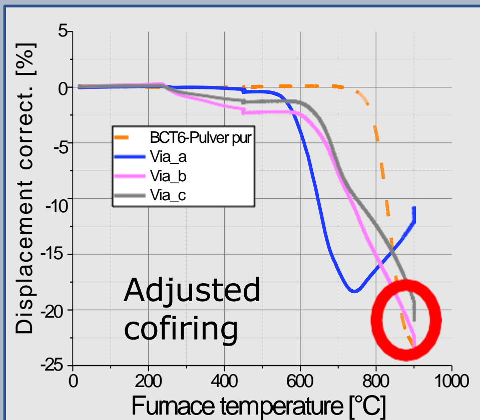


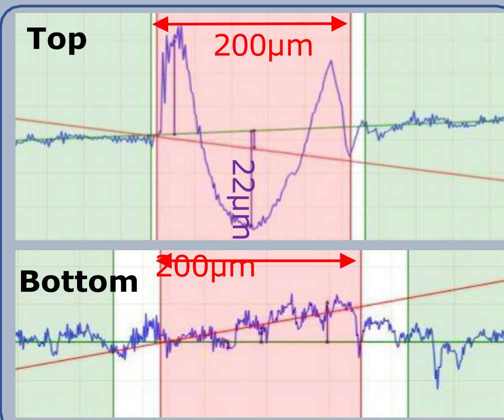




- Ag-based metallization for buried structures available
- Necessary print resolution achieved

Viafill





- Shrinkage matched to BCT6
- Processability confirmed
- Filling of 100 µm-Vias for 250 µm tape thickness possible

Further metal paste developments

- Transition-paste for mixed metal system (Au-Ag)
- Ag–Pd–Pt-solderable paste
- Polymer paste for Through-Silicon-Via Technology

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Sintering parameter, metallization system und release tape

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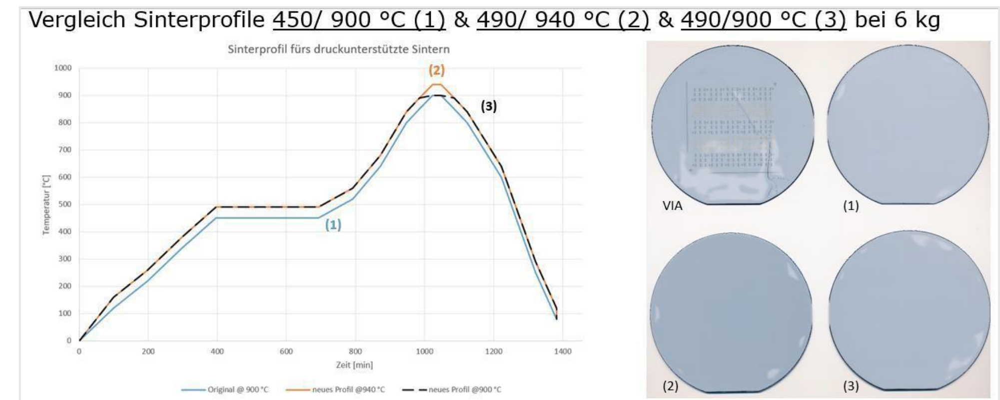
Systematic investigation of sinterparameter

- Adjusted burnout- & sintering temperature for pressure assisted sintering (6 kg – fixed weight)
- Profile (2) shows best results followed by profile (3)
- Pulltest to characterize bond interface

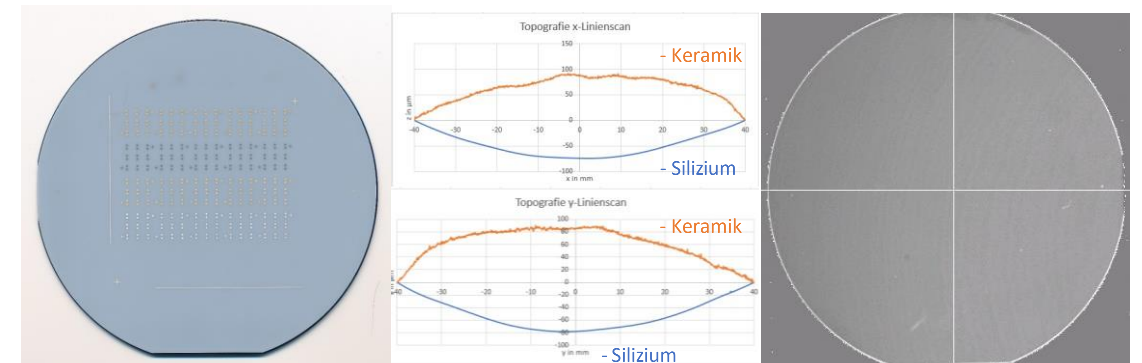


Influence of burnout & sintering temperature on the bond interface of BCT6 H066

Investigation of metallization and release tape interaction

- Combination of 4 release tapes and 4 metallization pastes (BCT6 H100)
- Releasetapes: IKTS F800, IKTS F1000, CeramTecA, Kerafol
- Pastes: QR 150[1], LL 509[1], 5740 A[1], 7454 B[2]

[1] DuPont, [2] Namics



Bow-measurement and US-microscopy in SiCer

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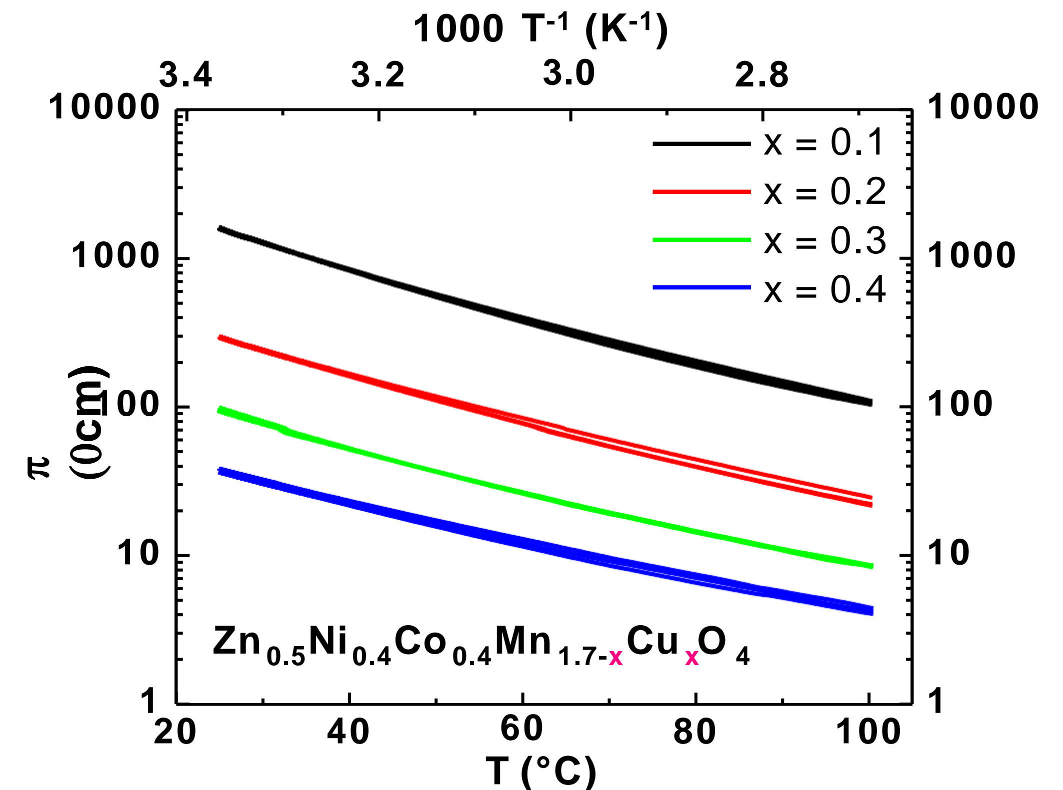
Developed within HIPS

Functional materials

- Magnetic shielding: $Ni_{0.5}Zn_{0.5}Fe_2O_4$ + 3 Ma.-% Bi_2O_3
- Inductive components: $Ni_{0.3}Cu_{0.2}Zn_{0.52}Fe_{1.98}O_{3.99}$
- Capacitor material: TiO_2 + 1 Ma.-% CuO
- NTC resistor: $Zn_{0.5}Ni_{0.4}Co_{0.4}Mn_{1.3}Cu_{0.4}O_4$

Paste composition

- Solid content: ≈ 70 Ma.-%
- Organics: ≈ 30 Ma.-%



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Screen printing on BCT 6

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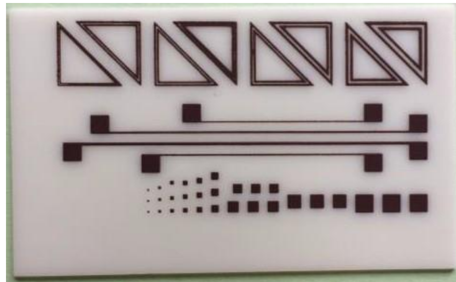
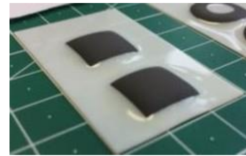
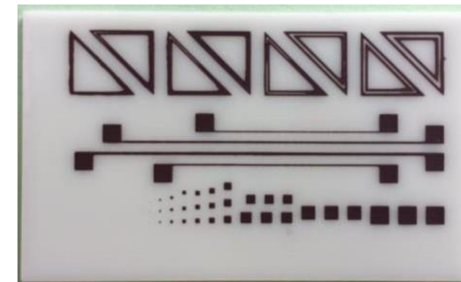
IKTS & EAH test structures

Funktion: **1.4.2 magn. shielding**


Postfiring

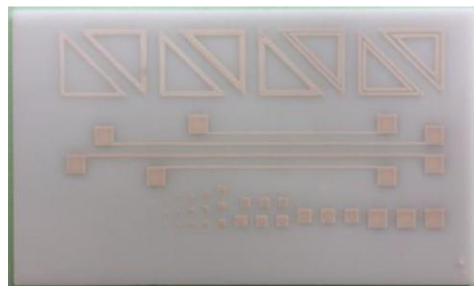

Cofiring

Funktion: **1.4.3 inductive components**


Postfiring

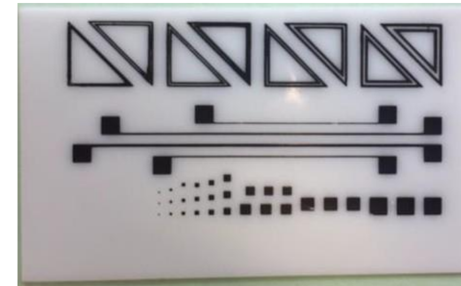
Cofiring

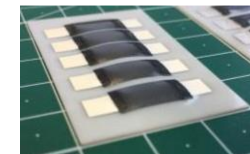
Funktion: **1.4.4 capacitor material**


Postfiring

Cofiring with
Ag-conductor (IKTS)

Funktion: **1.4.5 NTC resistors**


Postfiring


Cofiring with
Ag-conductor (IKTS)

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Structural elements

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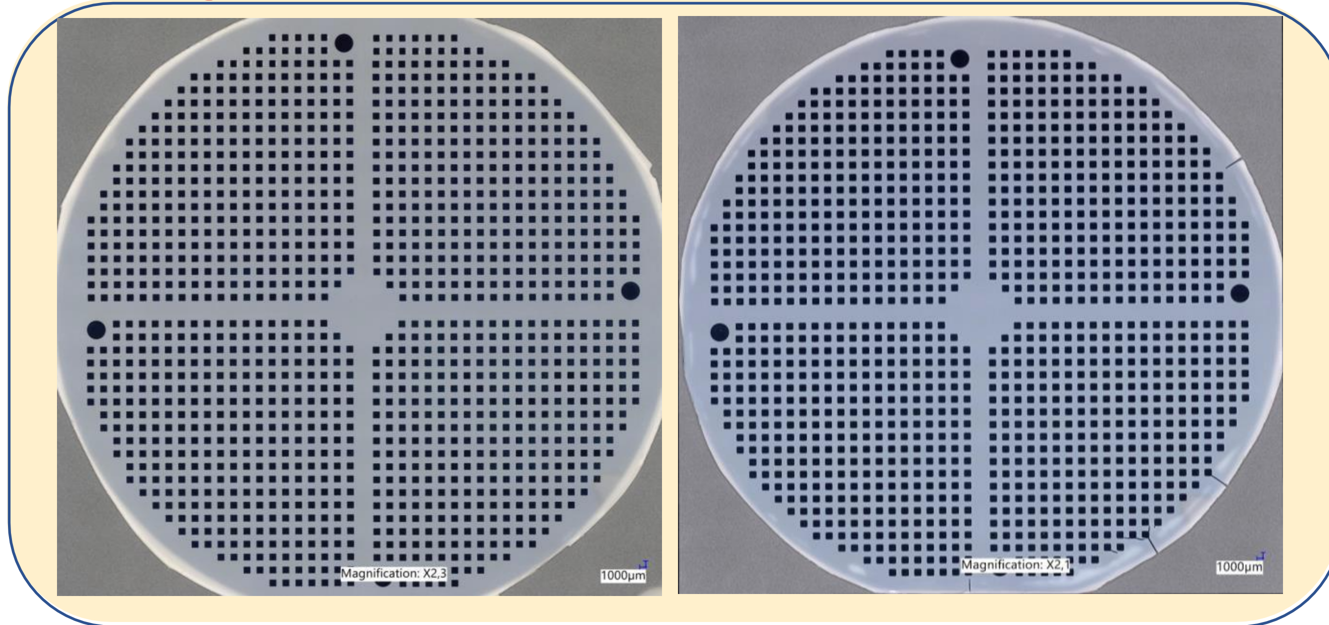
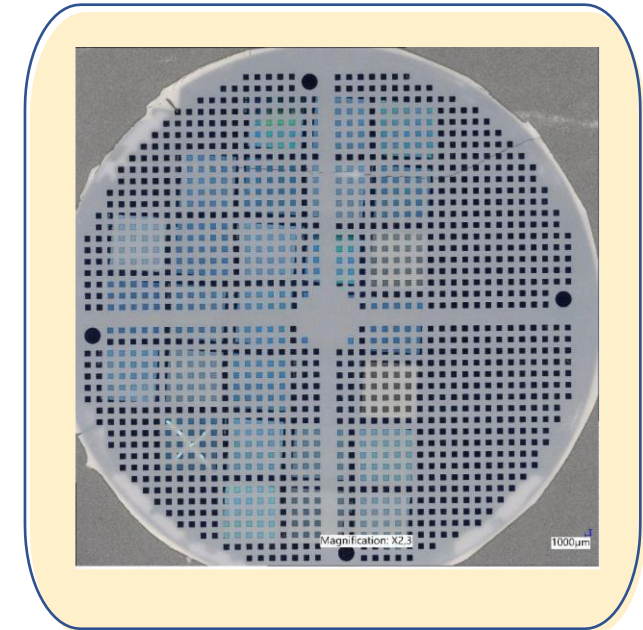
SiCer tests with open cavities in LTCC

11.5 kg **No weight**



- Crack-free SiCer with open cavities, 2DT
- Very good and uniform bonding
- IR sensor design 1.1 mm x 1.1 mm

Investigation of different Si-LTCC intefaces by laser surface activation



- Areas with better bonding behaviour were chosen for lasering of full wafer by LLT

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SiCer„electrostatic toolbox“ (5M - Concept), functional elements

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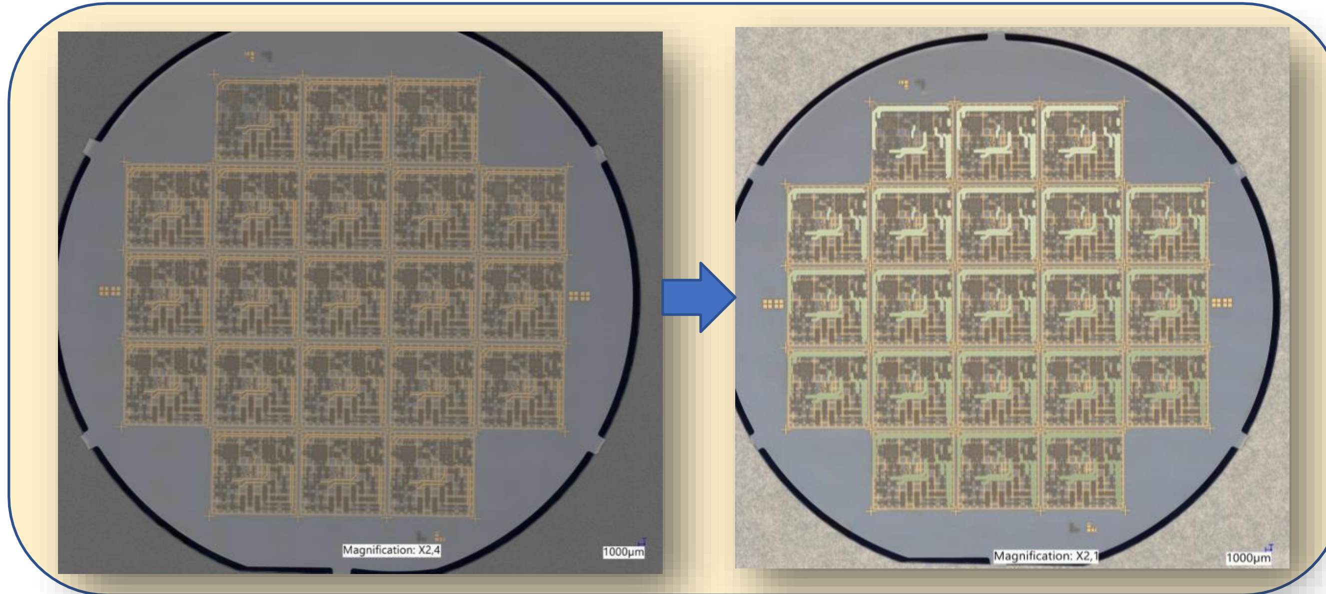
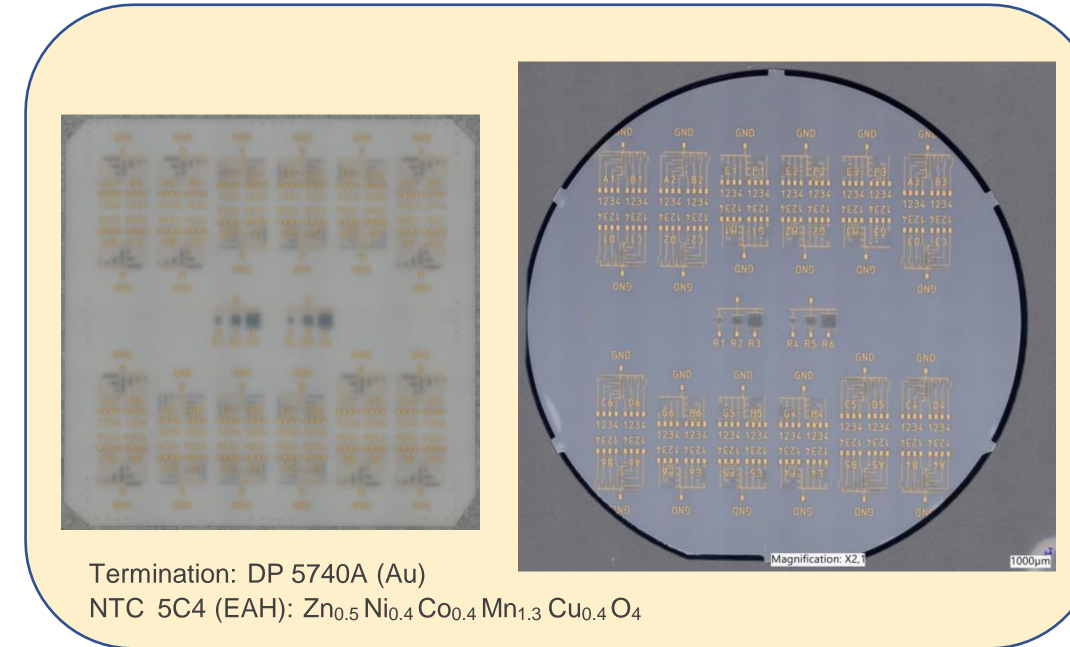
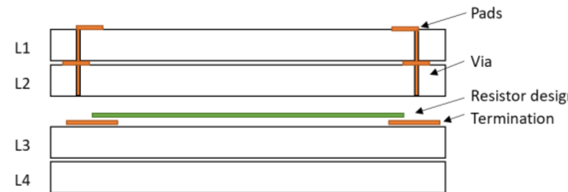




Termination: DP 5740A (Au)
NTC 5C4 (EAH): $Zn_{0.5}Ni_{0.4}Co_{0.4}Mn_{1.3}Cu_{0.4}O_4$

- 2 Double tapes
- Contact-pads (Au DP5740)
- Vias (Au DP5738R)
- Inner metallization (Au DP5740)
- Outer signal lines (Au DP5740)
- Outer solder pads (AuPt LL509)

Postfired glass as solder stop



Evaluation of NTC paste (from EAH) for T-sensors

- Constrained sintering,
- 2 DT 11.4 kg
- No crack or warpage

- SiCer,
- 2 DT 11.4 kg
- No crack or warpage

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CFD-simulation – impedance sensor (ILMSENS)

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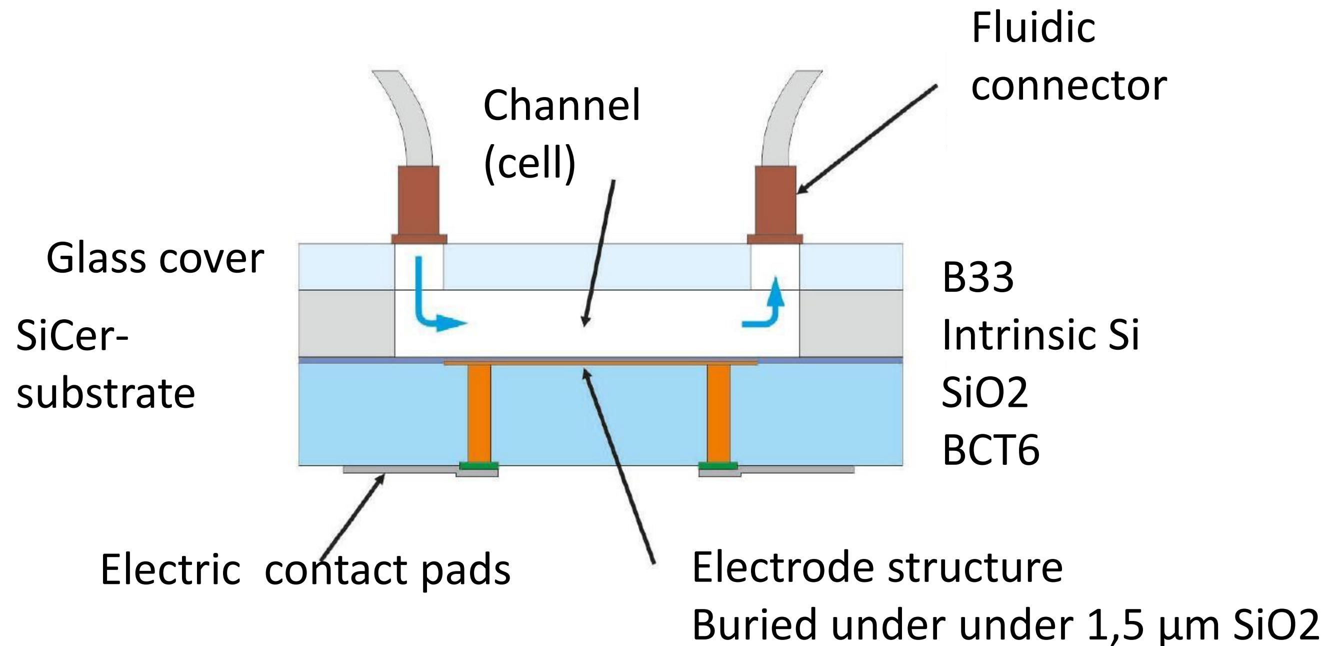
Objective of the simulation: Flow behavior of the liquid within the channel structure

Schematic:



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CFD-Simulation – Impedance sensor (ILMSENS)

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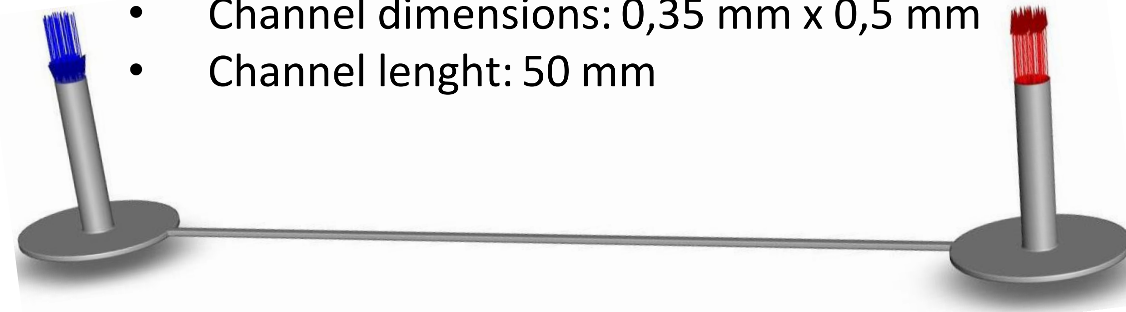
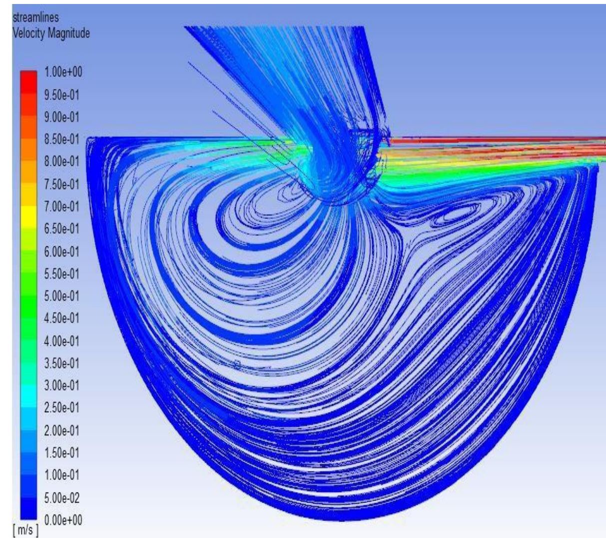
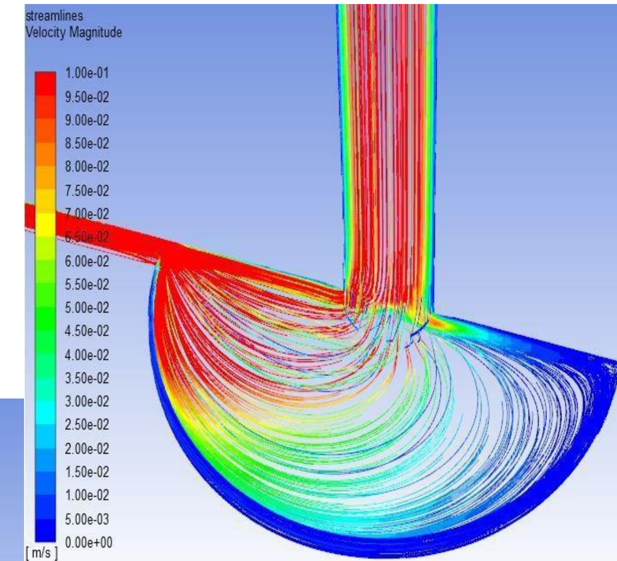
Fluidic configuratrion:

- Entrance/exit chamber: Ø 8mm
- Channel dimensions: 0,35 mm x 0,5 mm
- Channel lenght: 50 mm

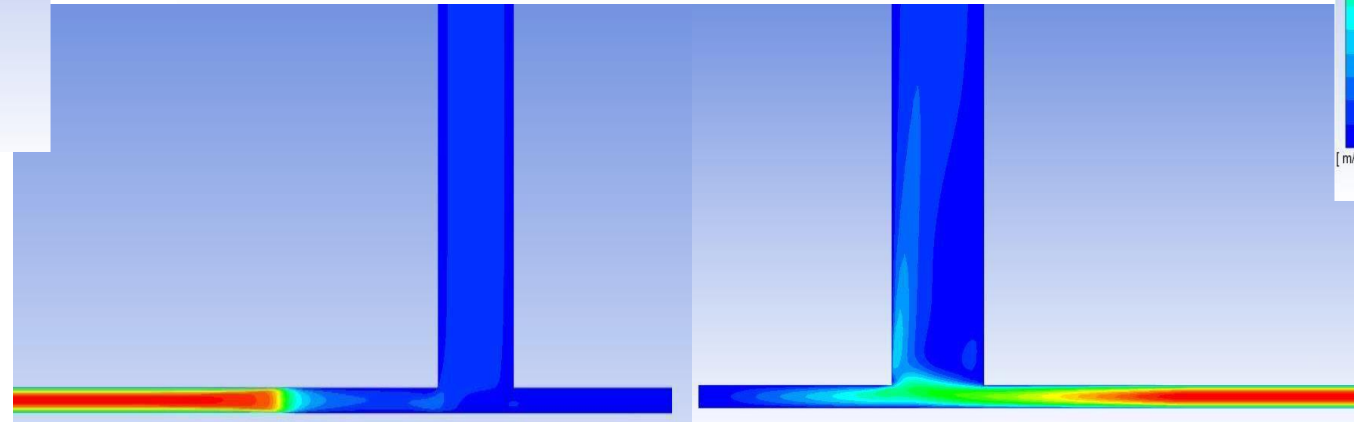




Flow simulation entrance



Flow simulation exit



Velocity profile entrance

Velocity profile exit

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Highlights CIS
Pressure sensor-wafer / pressure sintering

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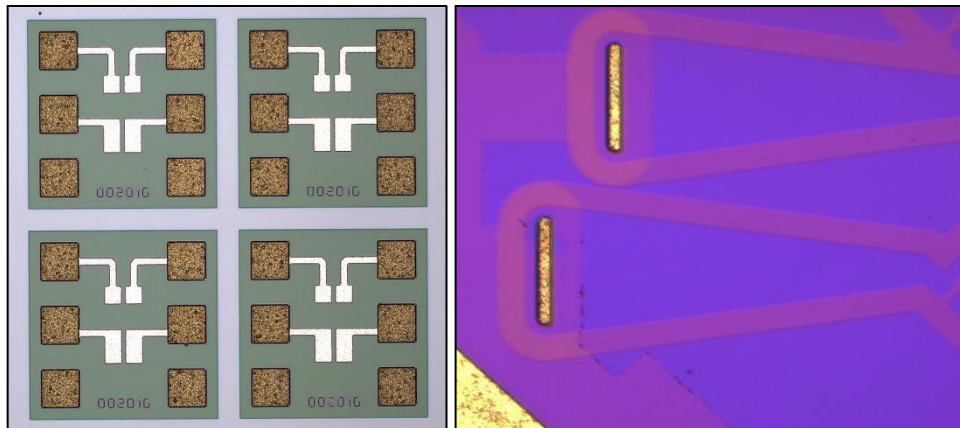
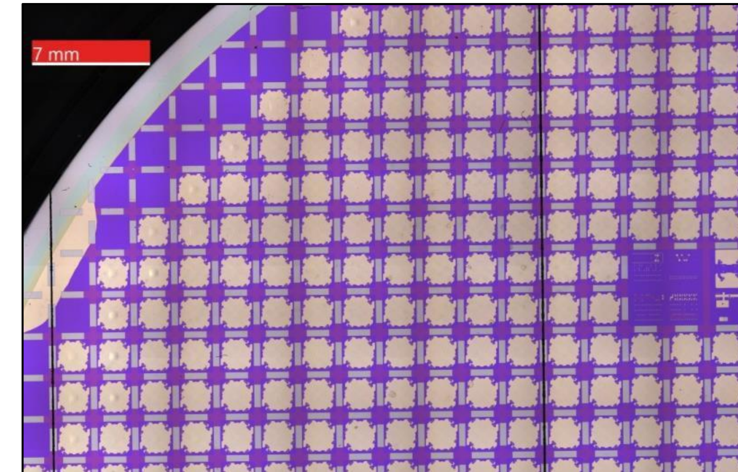
Process development together with TU Imenau

- Evaluation of refiring under pressure
- Evaluation of relaxation structures during pressure sintering
- Development and transfer to wafer level process with BCT ceramic
- SAM-Analysis + optical analysis:

➔ **SiCer composit substrate without visible cracks and displacements**





Wet chemical metallisation

- Test of maskless UBM
- Successful soldering on UBM (SAC)
- UBM compatible for geeignet für Flip-Chip-soldering
- Test of electrochemical metal deposition in the conctact hole ongoing

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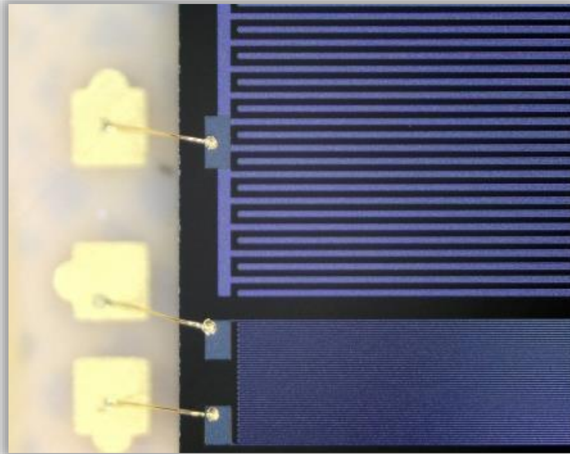
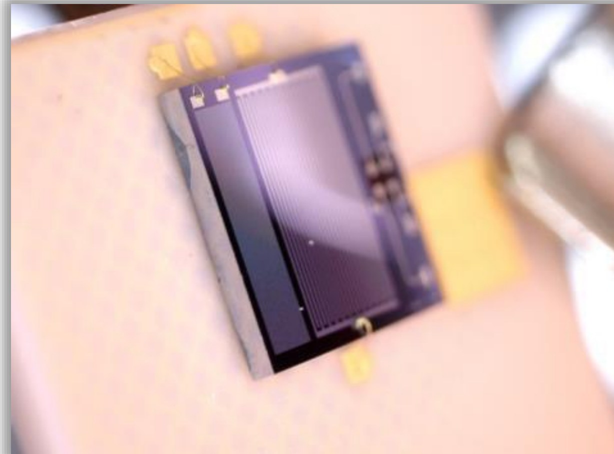
Highlights 5M
Wirebond-, Adhesive bonding and solder processes on SiCer modules

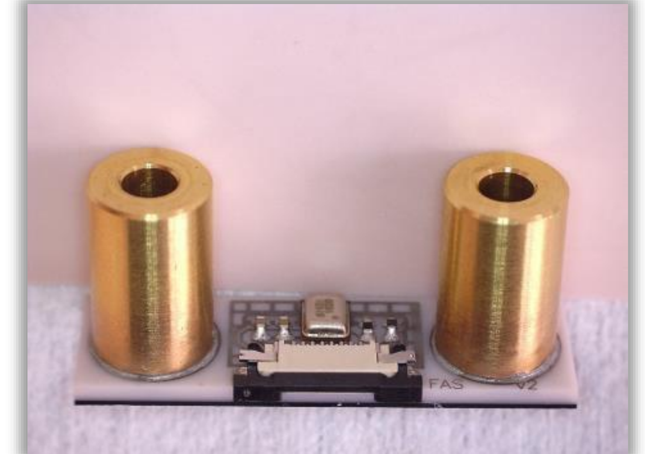
Reliable and established interconnection technologies on SiCer Substrates



Au wire bond between Si and ceramic side



Assembly of a Si Chip onto the ceramic side by adhesive bonding



Soldered connectors and SMD components on SiCer

5microns microsystem professionals
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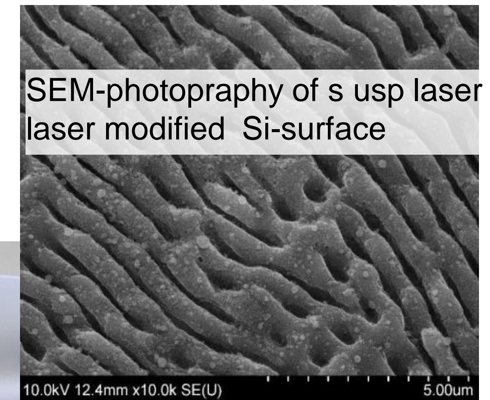
Ultrashort pulse (usp) laser micro-machining

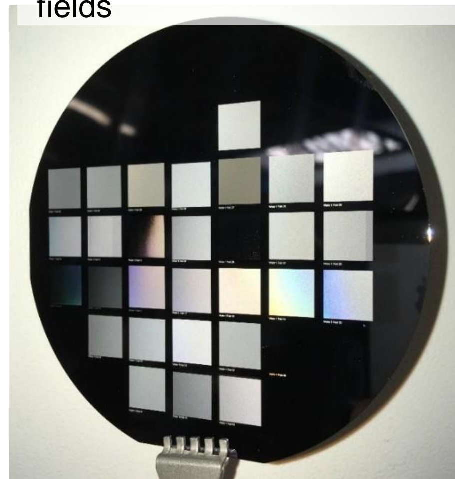
HIPS HIGH PERFORMANCE SENSORS
Powered by SiCer

- Plugged holes exactly adjusted to the depth of the Si on SiCer substrate ending at the ceramic surface to provide TSVs.)
  - Test drills in Si for metallisation tests (100, 150, 200 und 300µm) realised
  - Testwafer with plugged holes ending at ceramic part of the SiCer substrate realised

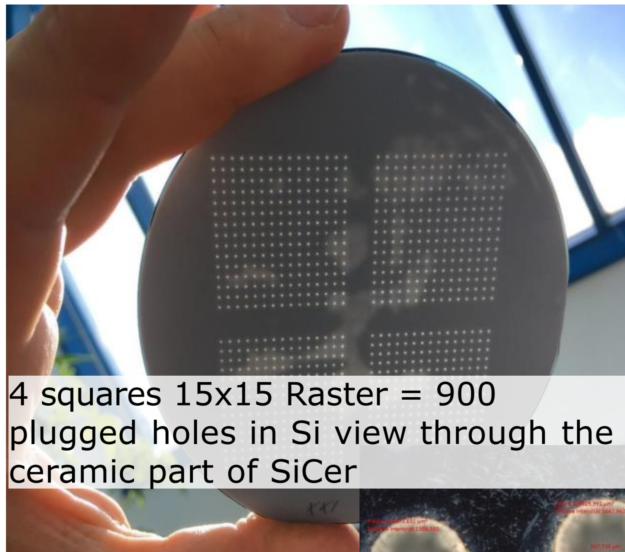


SEM-photopraphy of s usp laser laser modified Si-surface

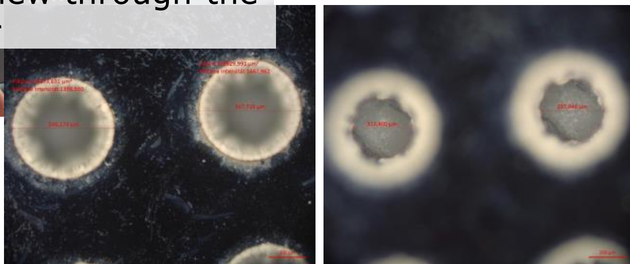
4“ Wafer with 30 parameter fields



4“ Testwafer mit 8 Parametervarianten



4 squares 15x15 Raster = 900 plugged holes in Si view through the ceramic part of SiCer



- Microstrucrures of Si-Wafers to activate the surface and enhance the bond interface between Si and ceramic

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3. Functionality and upscaling

- Structural and functional demonstrator elements in both LTCC and Si can be integrated
- USP laser processes for structural elements are developed and validated
- Cost efficient Ag-based metal paste for cofiring is developed and under evaluation
- TSV are developed and in verification
- Functional materials for SiCer integration are developed and under evaluation
- 2. generation tape material is developed an in evaluation
- Upscaling of the LTCC format from 4 to 6 Zoll is validated
- Upscaling of tape casting from batch casting to continuous casting is validated

Integrated structures and functions as well as first sensor elements are realised based on the SiCer technology platform

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The SiCer technology platform developed in the HIPS project offers mass production at highest performance

- **It Provides a maximum of integration density, complexity and functionality**
  - A thin film compatible Si side
  - Smallest MEMS und NEMS with integrated fluidic and functional elements
  - High resolution wiring
  - A thick film compatible ceramic side
  - Established interconnection technology and shortest signal lines from the sensor to the electronics

- **It performs with high reliability under extreme environmental conditions**
  - Cofire bond process up to 940°C and postfire process stability up to 600°C is justified
  - Matching of the TCE between LTCC und Si is verified

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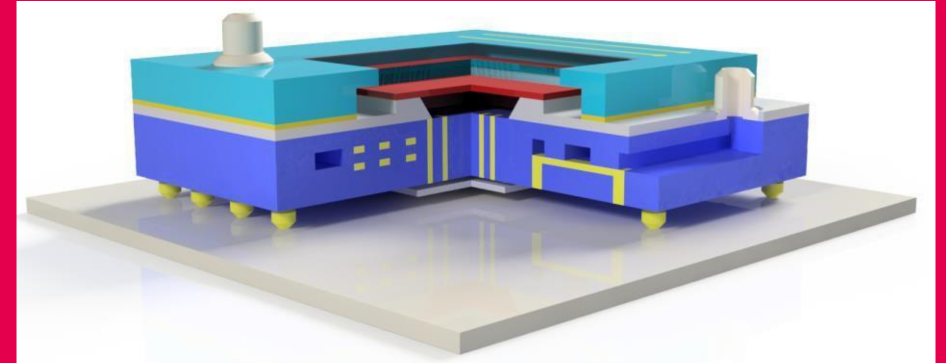
HIPS | HIGH PERFORMANCE SENSORS

Powered by SiCer - The best of both worlds



Thanks to the partners and to the VIA team contributing to the work, thank you for your attention.

Wachstumskern HIPS

HIGH-PERFORMANCE-SENSORSYSTEME durch Verbindung von Siliziumtechnologie und keramischer Mehrlagentechnik

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